Ministry of Higher Education
High Institute of Eng & Technology
Electronics and communication Dept.
Allowed Time: 75 Minutes
Course: Integrated Circuits

Date: -11- 2017
Mid Term examination
Code: CEC404
Total Grad : 20 Mark
Examiner: Dr. Bedir Yousif

*The Exam in one page
* Any missing data could be reasonably assumed

*Books & notes not allowed

Solve All Questions: (20 Mark)

a- What is an integrated circuits and its advantages over a circuits made by interconnecting a discrete components? (3 Marks)

b- Sate the main differences between monolithic and hybrid technologies used with ICs? (3 Marks)

c- State the advantages and features of four group logic families digital ICs? (3 Marks)

d- State the simplified process sequence for the fabrication of the n-well CMOS integrated circuit with a single polysilicon layer, showing only major fabrication steps? (3 Marks)

e- define: Moore's law - Lithography process - Transient response for an inverter with a rectangular input waveform.? (3 Marks)

f- Drive an expression for the total power dissipated in a digital integrated circuits? (2 Marks)

g- Find the inverter dissipation power, logic swing, Noise margin and sketch the VTC if (3 Marks)

R_D= 25 KΩ
V_{OH} = 1.8 V
V_{OL} = 0.12 V
V_{IL} = 0.59 V
V_{IH} = 1.06 V
For inverter illustrated in Fig. 1.

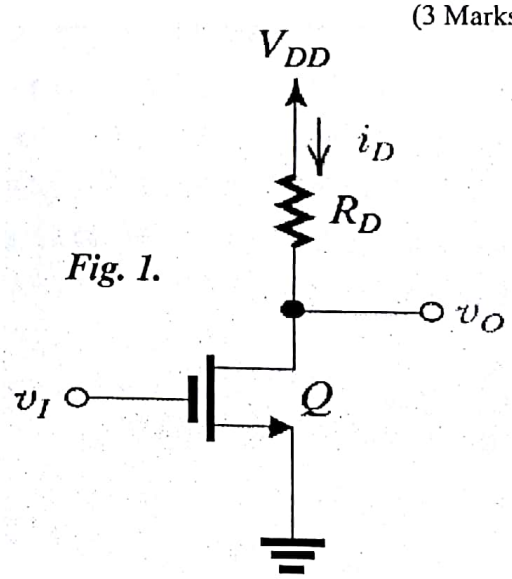


Fig. 1.

Best wishes of success
Dr. Bedir yousif

Solution

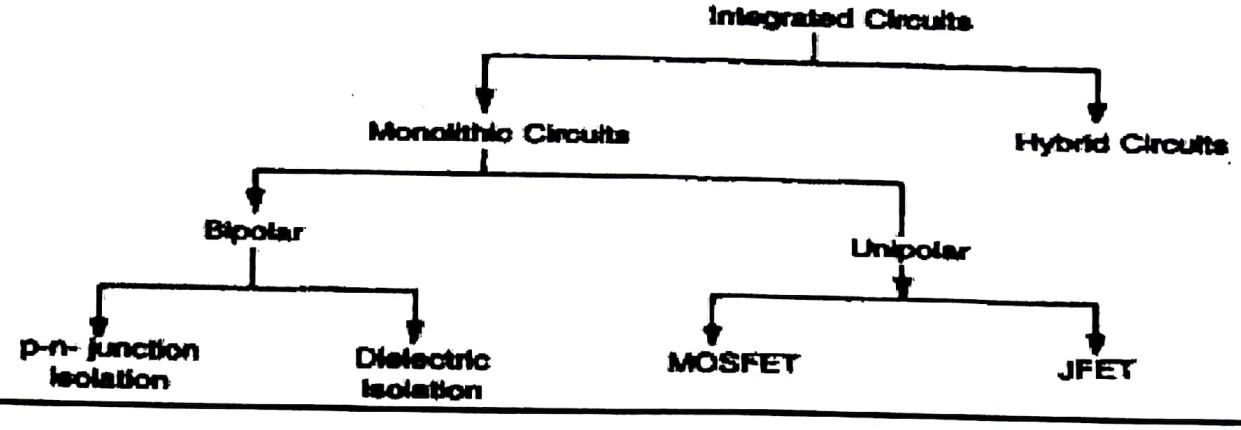
-a-

The integrated circuit or IC is a miniature, low cost electronic circuit consisting of active and passive components that are irreparably joined together on a single crystal chip of silicon. Most of the

1. Miniaturization and hence increased equipment density
2. Cost reduction due to batch processing
3. Increased system reliability due to elimination of soldered joints
4. Improved functional performance (as it is possible to fabricate even complex circuits for better characteristics)
5. Matched devices
6. Increased operating speeds (due to the absence of parasitic capacitance effect)
7. Reduction in power consumption.

b- Sate the main differences between monolithic and hybrid technologies used with ICs?

In monolithic integrated circuits, all circuit components, both active and passive elements and their interconnections are manufactured into or on top of a single chip of silicon. The monolithic circuit is ideal for applications where identical circuits are required in very large quantities and hence provides lowest per-unit cost and highest order of reliability. In hybrid circuits, separate component parts are attached to a ceramic substrate and interconnected by means of either metallization pattern or wire bonds. This technology is more adaptable to small quantity custom circuits. Based upon the active devices used, ICs can be classified as bipolar (using BJT) and unipolar (using FET). Bipolar and unipolar ICs may further be classified depending upon the isolation technique or type of FET used as in Fig. 1.1.



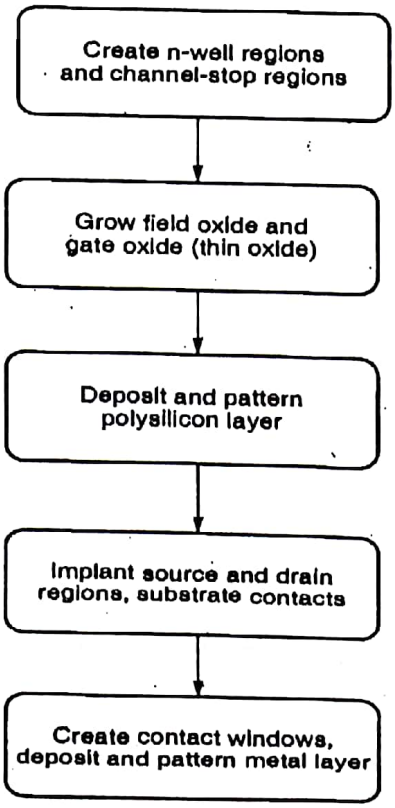
c- State the advantages and features of four group logic families digital ICs? (3 Marks)

1- MOS logic circuits are by far the most important today. They draw their name from the silicon MOSFETs on which they are based. The two important variations are NMOS, which uses n-channel MOSFETs exclusively, and CMOS, which uses p-channel and n-channel MOSFETs in complementary pairs. CMOS is used almost exclusively in modern microprocessors and application-specific integrated circuits (ASICs). The unique advantage of CMOS is the low standby power dissipation.

2- Saturated bipolar logic families include resistor–transistor logic (RTL), diode–transistor logic (DTL), and the many families of transistor–transistor logic (TTL). A common feature of these circuits is that they use silicon bipolar transistors as saturated switches. Their advantage is that bipolar transistors exhibit higher transconductance than MOSFETs. Therefore, although these circuits are inherently slower than CMOS, they are less susceptible to capacitive loading. The result is that saturated bipolar gates can outperform CMOS in applications involving large-load capacitances such as motherboards.

3- Nonsaturated bipolar logic families are collectively called emitter-coupled logic (ECL). ECL gates are the fastest silicon digital circuits with regard to off-chip propagation delays and outperform saturated bipolar circuits by a considerable margin. Consequently, they are important in high-performance computing and high data-rate digital communications. In addition, the possible development of ECL circuitry using SiGe alloys or compound semiconductors may further boost the performance of ECL.

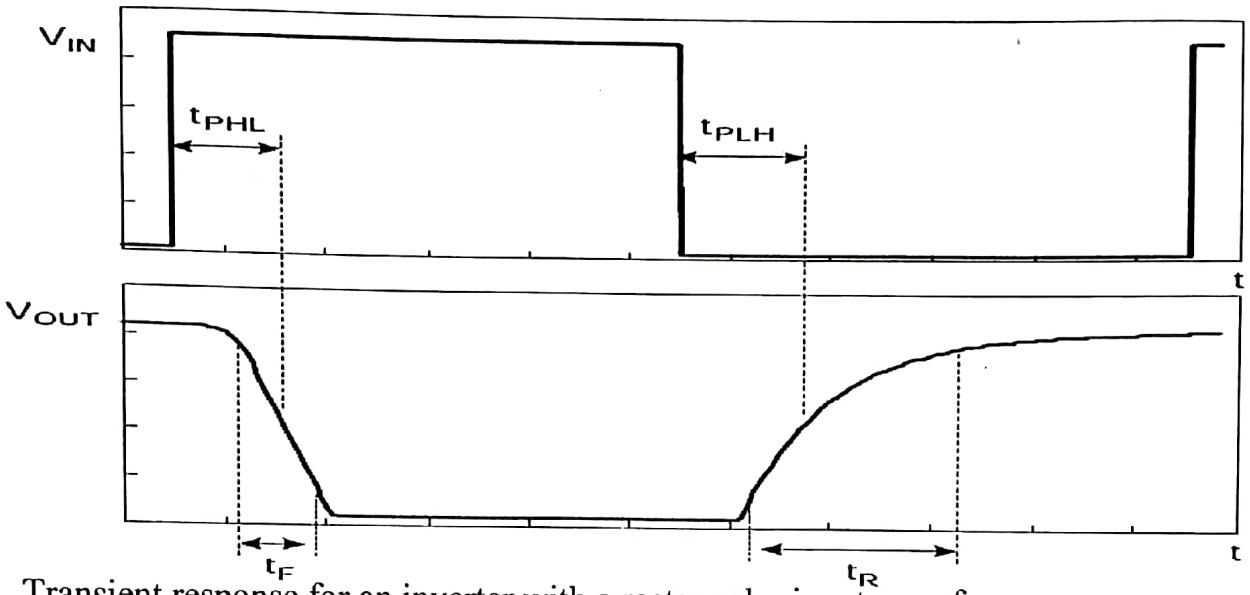
4-compound semiconductor logic families such as GaAs direct coupled FET logic (DCFL) are used only in niche applications that demand higher speed than is available from silicon. These include digital communication and, occasionally, microprocessors.



Q1-d

"Moore's law" states that the number of transistors per chip doubles every 18 months.

The process used to transfer a pattern to a layer on the chip is called *lithography*. Since each layer has its own distinct patterning requirements, the lithographic sequence must be repeated for every layer, using a different mask.



Transient response for an inverter with a rectangular input waveform.

The four important transient parameters for the inverter are the low-to-high propagation delay, t_{PLH}, the high-to-low propagation delay, t_{PHL}, the output rise time, t_R, and the output fall time, t_F.

The rise time and fall time for the output are measured between the 10 and 90% points on the waveform. The 10% point is the point in time at which the output voltage is 1/10 of the way from the low value to the high value; the 90% point is defined in similar fashion. The propagation delays are measured between the 50% points on the input and output waveforms (the points at which the voltage is midway between the two limiting values). As a matter of nomenclature, the low-to-high propagation delay, t_{PLH}, refers to the low-to-high transition at the output node. For an inverter, this corresponds to the opposite transition at the input node. Similarly, t_{PHL} refers to the high to- low transition at the output node. Often the two propagation delays are very different and should be specified. In other situations, the transient response is entirely symmetric so that the two propagation delays are equal. In such cases it suffices to use the notation t_P.

e-

$$p_{DD}(t) = V_{DD} i_D(t)$$

The energy delivered by the power supply to charge the capacitor can be determined by integrating $p_{DD}(t)$ over the charging interval T_c,

$$E_{DD} = \int_0^{T_c} V_{DD} i_D(t)\, dt$$

$$= V_{DD} \int_0^{T_c} i_D(t)\, dt$$

$$= V_{DD} Q$$

where Q is the charge delivered to the capacitor during the charging interval. Since the initial charge on C was zero,

$$Q = CV_{DD}$$

Thus,

$$E_{DD} = CV_{DD}^2$$

Since at the end of the charging process the energy stored on the capacitor is

$$E_{\text{stored}} = \frac{1}{2} CV_{DD}^2$$

we can find the energy dissipated in the pull-up switch as

$$E_{\text{dissipated}} = E_{DD} - E_{\text{stored}} = \frac{1}{2} CV_{DD}^2$$

$$E_{\text{dissipated}} = \frac{1}{2} CV_{DD}^2$$

This amount of energy is dissipated in the on-resistance of switch P_D and is converted to heat.

Thus in each cycle of inverter switching, an amount of energy of $\frac{1}{2}CV_{DD}^2$ is dissipated in the pull-up switch and $\frac{1}{2}CV_{DD}^2$ is dissipated in the pull-down switch, for a total energy loss per cycle of

$$E_{\text{dissipated}}/\text{cycle} = CV_{DD}^2$$

If the inverter is switched at a frequency of f Hz, the dynamic power dissipation of the inverter will be

$$P_{\text{dyn}} = f CV_{DD}$$

static power or DC power dissipated is $P_{DC} = \frac{P_L + P_H}{2}$

$$P_L = V_{DD} I_{DDL}$$
$$P_H = V_{DD} I_{DDH}$$

the total power dissipation is

$$P = P_{DC} + P_{\text{dyn}}$$

f- LS= 1.8-0.12 = 1.68 V

$N_{ML} = V_{IL} - V_{OL} = 0.47$ V

$N_{MH} = V_{OH} - V_{IH} = 0.74$ V

The inverter dissipates power only when the output is low, in which case the current drawn from the supply is

$$I_{DD} = \frac{V_{DD} - V_{OL}}{R_D} = \frac{1.8 - 0.12}{25\ \text{k}\Omega} = 67\ \mu\text{A}$$

and the power drawn from the supply during the low-output interval is

$$P_D = V_{DD} I_{DD} = 1.8 \times 67 = 121\ \mu\text{W}$$

Since the inverter spends half of the time in this state,

$$P_{D\text{average}} = \frac{1}{2} P_D = 60.5\ \mu\text{W}$$