معالجة الإشارات

Q1.A. Advantages of digital as opposed to analogue signal processing include the following

(*choose 4*) :-

- More and more signals are being transmitted and /or stored in digital form so it makes sense to process them in digital form also.
- DSP systems can be designed and tested in "simulation " using universally available computing equipment (e.g. PCs with sound and vision cards).
- Guaranteed accuracy, as pre-determined by word-length and sampling rate.
- Perfect reproducibility. Every copy of a DSP system will perform identically.
- The characteristics of the system will not drift with temperature or ageing.
- Advantage can be taken of the availability of advanced semiconductor VLSI technology.
- DSP systems are flexible in that they can be reprogrammed to modify their operation without changing the hardware. Products can be distributed / sold and updated via Internet.
- Digital VLSI technology is now so powerful that DSP systems can now perform functions that would be extremely difficult or impossible in analogue form. Two examples of such functions are :(i) adaptive filtering (where the parameters of a digital filter are variable and must be adapted to the characteristics of the input signal) and, (ii) speech recognition which is again based on information obtained from speech by digital filtering.

Disadvantages of digital signal processing (*choose one*) :

- DSP designs can be expensive especially for high bandwidth signals where fast analogue/digital conversion is required.
- The design of DSP systems can be extremely time-consuming and a highly complex and specialized activity. There is an acute shortage of electrical engineering graduates with the knowledge and skill required.
- The power requirements for DSP devices can be high, thus making them unsuitable for battery powered portable devices such as mobile telephones. Fixed point processing devices (offering integer arithmetic only) are available which are simpler than floating point devices and less power consuming. However the ability to program such devices is a particularly valued and difficult skill.

Q1.B **odd function so all a_n terms are zero**

Q2.A.. .(a) Considering first the DTFT formula:

$$X(e^{j\Omega}) = \sum_{n=-\infty}^{\infty} x[n]e^{-jn\Omega} \quad \text{where } \Omega = \omega / f_s = \omega T \text{ radians/sample}$$

This transforms a (possibly complex) discrete time signal {x[n]} of infinite duration to the relative frequency (Ω) domain.

Defining: $X(e^{j\Omega_k})=X[k]$, the DFT transforms a finite (possibly complex valued) sequence $\{x[n]\}_{0,N-1}$ to the finite complex valued sequence $\{X[k]\}_{0,N-1}$.
The DFT formula is:-

$$X[k]=\sum_{n=0}^{N-1}x[n]e^{-j\Omega_k n} \text{ where } \Omega_k=2\pi k/N \text{ for } k=0,1,2,.....,N-1$$

For each k = 0,1, 2, ..., N-1, X[k] is a sample of the spectrum $X(e^{j\Omega})$ at $\Omega=2\pi k/N$. In this case, $X(e^{j\Omega})$ is the spectrum (DTFT) of an infinite discrete time signal $\{x[n]\}$ comprising $\{x[n]\}_{0,N-1}$ padded out to infinity (in both directions) with zeros.
Therefore Ω is in the range 0 to 2π is and $X(e^{j\Omega})$ is uniformly sampled over this range.

Q2.b State and prove the linear property of FT.

Stt:

$$F[af(x)+bg(x)]=aF[s]+bG[s]$$

Proof:

$$F[f(x)] = F[s] = \frac{1}{\sqrt{2\pi}}\int_{-\infty}^{\infty} f(x)e^{isx}\,dx$$

$$F[af(x)+bg(x)] = \frac{1}{\sqrt{2\pi}}\int_{-\infty}^{\infty}[af(x)+bg(x)]e^{isx}\,dx$$

$$= \frac{1}{\sqrt{2\pi}}\int_{-\infty}^{\infty} af(x)\,e^{isx}\,dx + \frac{1}{\sqrt{2\pi}}\int_{-\infty}^{\infty} bg(x)\,e^{isx}\,dx$$

$$= \frac{a}{\sqrt{2\pi}}\int_{-\infty}^{\infty} f(x)\,e^{isx}\,dx + \frac{b}{\sqrt{2\pi}}\int_{-\infty}^{\infty} g(x)\,e^{isx}\,dx$$

$$=aF[s]+bG[s]$$

4. **Find the Fourier transform of** $f(x)=\begin{cases}1-|x| & \text{if } |x|<1\\ 0 & \text{if } |x|>1\end{cases}$ **. Hence deduce that**

$$\int_0^{\infty}\left(\frac{\sin t}{t}\right)^4 dt=\frac{\pi}{3}$$

Solution

Fourier transform

$$F[f(x)]=\frac{1}{\sqrt{2\pi}}\int_{-\infty}^{\infty} f(x)e^{isx}dx$$

$$=\frac{1}{\sqrt{2\pi}}\int_{-1}^{1}(1-|x|)e^{isx}dx$$

$$=\frac{2}{\sqrt{2\pi}}\int_{0}^{1}(1-|x|)\cos sx\,dx$$

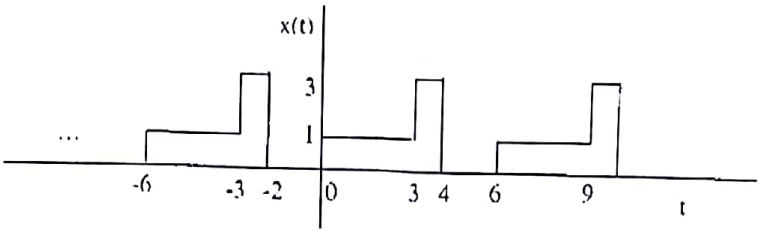
$$=\sqrt{\frac{2}{\pi}}\left((1-x)\frac{\sin sx}{s}-(-1)\left(\frac{-\cos sx}{s^2}\right)\right)_0^1$$

$$=\sqrt{\frac{2}{\pi}}\left(\frac{-\cos sx}{s^2}+\frac{1}{s^2}\right)$$

$$F(s)=\sqrt{\frac{2}{\pi}}\left(\frac{1-\cos sx}{s^2}\right)$$

By parseval's identity, $\int_{-\infty}^{\infty}|F(s)|^2 ds=\int_{-\infty}^{\infty}|f(x)|^2 dx$

$$\int_{-\infty}^{\infty}|f(x)|^2 dx=\int_{-1}^{1}(1-|x|)^2 dx\quad 2\int_{0}^{1}(1-x)^2 dx\quad =-\frac{2}{3}\left[(1-x)^3\right],$$



$$x(t) = \sum_{n=-\infty}^{\infty} C_n e^{jn\omega_0 t} \qquad T = 6,\ \omega_0 = \frac{2\pi}{6} = \frac{\pi}{3}$$

$$C_n = \frac{1}{6}\int_0^6 x(t) e^{-jn\omega_0 t}\,dt$$

$$= \frac{1}{6}\int_0^3 e^{-jn\frac{\pi}{3}t}\,dt + \frac{1}{6}\int_3^4 e^{-jn\frac{\pi}{3}t}\,dt$$

$$= \frac{1}{6}\frac{-1}{j\pi/3n} e^{-jn\frac{\pi}{3}t}\Big|_0^3 + \frac{1}{2}\frac{-1}{jn\pi/3} e^{-jn\pi/3\,t}\Big|_3^4, \quad n\neq 0$$

$$C_n = \frac{-1}{j2\pi n}\left(e^{-jn\pi} - 1\right) - \frac{3}{j2\pi n}\left(e^{-jn4\pi/3} - e^{-jn\pi}\right), \quad n\neq 0$$

if $n=0$, $C_0 = \frac{1}{6}\int_0^6 x(t)\,dt = 1$

Q1.B.

Q3.A.

Comparison of IIR and FIR digital filters:

<u>IIR type digital filters</u> have the advantage of being economical in their use of delays, multipliers and adders.

[1]

They have the disadvantage of being sensitive to coefficient round-off inaccuracies and the effects of overflow in fixed point arithmetic. These effects can lead to instability or serious distortion.

[1]

Also, an IIR filter cannot be exactly linear phase.

[1]

FIR type digital filters may be realised by non-recursive structures which are simpler and more convenient for programming especially on devices specifically designed for digital signal processing.

These structures are always stable, and because there is no recursion, round-off and overflow errors are easily controlled.

A FIR filter can be exactly linear phase.

[1]

The main disadvantage of FIR filters is that large orders can be required to perform fairly simple filtering tasks.

[1]

Q3.c.

Zeros do not affect stability.

Poles must lie inside unit circle for stability.

Gain response determined by the "distance rule":-

$y[n]=x[n]+1.21x[n-2]-0.8y[n-1]$

$$H(z)=\frac{1+1.21z^{-2}}{1+0.8z^{-1}}=\frac{z^2+1.21}{z(z+0.8)}=\frac{(z-1.1j)(z+1.1j)}{z(z+0.8)}$$

Zeroes at z = -1.1j and z = +1.1j Poles at z = 0 and z = -0.8

Filter is causal as impulse response will be zero for n<0.

Filter is stable as poles are inside unit circle.

Q2.A Choose and explain the correct answer

1. Which is known as flash converter?

a. Weighted resistor D/A converter

b. Parallel A/D converter

c. Stair step A/D converter

d. Up – down counter type A/D converter

Soln. (b)

Flash ADC is the fastest of all D/A converters and uses 2n-1 comparators. It is expansive

2. Which converters use integrating op-amp

a. Parallel A/D converter

b. Single slope A/D converter

c. Dual slop A/D converter

d. Both (b) and (c)

Soln. (c)

The core of the dual slope A/D converter is the integrating op-amp and thus it has good noise immunity and its accuracy is high. It requires 2.2n twice the ramp type clock cycles for conversion.

3 . The accuracy of A/D conversion is generally

a. ±12 LSB

b. ± LSB

c. ± 54 LSB

d. None of the above

Soln. (a)

It is half of the resolution of A/D converter

6. The number of counter states which an 8 bit stair step A/D converter has to pass through before conversion is

a. 1

b. 8

c. 255

d. 256

Soln. (d)

The number of counter states for 8 bit ramp type A/D converter is 28 = 256

7. An n bit ADC using V as reference has a resolution of

a. $V2n$

b. $V(n)$

c. $V2n-1$

d. 2 V (n)

Soln. (c)

Each successive binary count is equal to $12n-1$ of the total, so the resolution of n bit ADC using V as reference is $V2n-1$

8. A 6 bit ladder D/A converter has input 101001. For 1 = 10 V and 0 = 0V, The output is

a. 4.23

b. 6.51

c. 5.52

d. 9.23

Soln. (b)

For a 6 bit D/A converter whose output varies from 0 to 10V, the resolution is Res=1026−1=1063=0.1587

The resolution is the smallest analog change in the output or a change in one LSB So $101001=(41)10$
So output is $41\times0.1587=6.51V$

9. A 10 bit D/A converter given a maximum output of 10.23V. The resolution is

a. 10 mV

b. 20 mV

c. 15 mV

d. 25 mV

Soln. (a)
Resolution $10.23210-1=10.231023=1100\ volts=10mv$
Q2.B.For an ADC, match the following : if

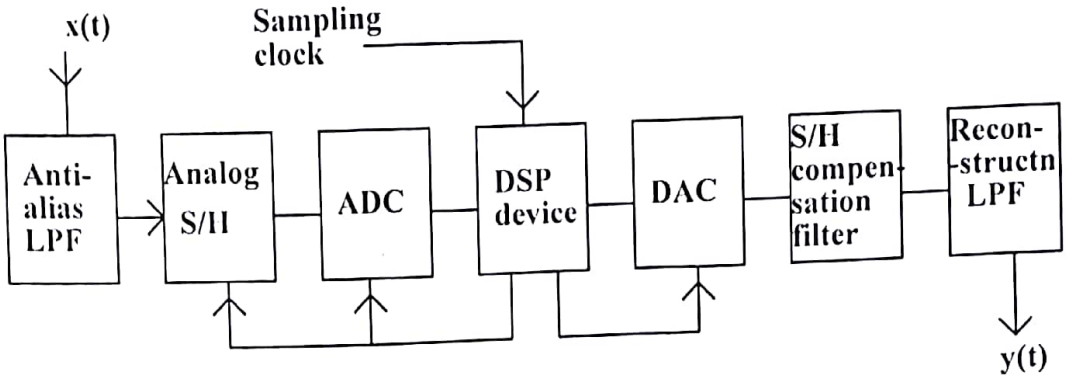
List 1	List2
(a) Flash converter (b) Dual slope converter (c) Successive approximation converter	(1) Requires a conversion time of the order of a few seconds (2) Requires a digital-to-analog converter (3) Minimizes the effect of power supply interference. (4) Requires a very complex hardware (5) Is a tracking A/D converter.

Soln. Flash converter or parallel A/D converter is fastest of all but requires a complex hardware. Dual slope integrator has good noise immunity and thus minimizes the effect of power supply interference. Successive approximation has shorter conversion time of the order of μsec and depends upon the number of bits only. For n bit ADC, it requires n clock cycles. It uses D/A converter.
A – 4, B – 3, C – 2

Q2.c

Vin at the non inverting terminal = 18 + 12 = 58
$V0 = (1 + Rf\ R)\ Vin = 8 \times 58 = 5V$

Q1.c Block diagram of a typical DSP system for processing analogue signals:



Antialiasing LPF: Analogue low-pass filter with cut-off frequency less than half the sampling frequency (fs) to remove (strictly, to sufficiently attenuate) any spectral energy of the input signal x(t) above fs/2. When x(t) is sampled, this spectral energy would otherwise produce, by aliasing, lower frequency energy capable of distorting the digitised input signal in the frequency range 0 to fs/2 . [1]

Analogue S/H:The analogue S/H circuit holds the input steady while the A/D conversion process takes place. [1]

ADC: Converts from analogue voltages to binary numbers of a specified wordlength. Quantisation error incurred. Samples taken at the "sampling frequency" *fs*. [1]

DSP device: Digital processing system. Normally controls S/H and ADC to determine sampling rate which is normally fixed by a sampling clock connected via an input port to the processor. The processor reads samples from the ADC when they become available, processes them and outputs the resulting samples to the DAC. Many special-purpose DSP devices (microprocessors) have been designed specifically for this type of processing. [1]

DAC: Converts from binary numbers output by the processor to analogue voltages. "Zero order hold" or "stair-case like" waveforms are normally produced. [1]

S/H compensation: Zero order hold reconstruction multiplies the spectrum of the true output by sinc(pi f/fs) which drops to about 0.64 at fs/2. Hence we lose up to -4 dB. The S/H filter compensates for this effect by boosting the spectrum

as it approaches fs/2. Can be done digitally before the DAC or by an analogue filter after the DAC. [1]

Reconstruction LPF: Removes "images" of -fs/2 to fs/2 band produced by S/H reconstruction. Spec similar to that of input filter. [1]